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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,865	12/05/2003	En-Hsing Chen	023-0029	8494

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EXAMINER	
NGUYEN, VAN THU T	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 12/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Supplemental **Advisory Action Before the Filing of an Appeal Brief**	**Application No.** 10/729,865	**Applicant(s)** CHEN ET AL.	
	Examiner VanThu Nguyen	**Art Unit** 2824	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 28 November 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1,27 and 28*.
   Claim(s) withdrawn from consideration: *2-20,22,23,29-60*.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

VanThu Nguyen
Primary Examiner
Art Unit: 2824

Continuation of 11. does NOT place the application in condition for allowance because: Applicants argue that dummy transistors DG2 and DG4 cannot be seen as selection devices because they do not connect the NAND strings to any kind of memory array node (e.g. global array line, main bit line, bias node, source line, etc.). Examiner disagrees with this statement for the following reasons:

Tatsukawa cites, in column 7, lines 29-61, and FIG. 1:

> "Sub-source line SSL1 is connected to a source line SL1 via source-side block select transistor SGS1 made conductive in response to source-side block select signal SS1. This source line SL1 is connected to a source-side *dummy transistor DG2 made conductive on in response to a drain-side block select signal SG2 [SD2?]*. One conduction node (drain) of dummy transistor DG2 is set to the open state.
>
> ...
>
> Sub-source line SSL2 is connected to a source line SL2 via source-side block select transistor SGS2 made conductive in response to source-side block select signal SS2. This source line SL2 is connected to a source-side *dummy transistor DG4 receiving a drain-side block select signal SG1 [SD1?] on its gate*. One conduction node (drain) of dummy transistor DG4 is set to the open state. *With no channel resistance of the dummy transistor, a resistance between the sub-source line and the source line can be small.*
>
> *These dummy transistors DG1-DG4 are employed so that sub-bit lines SBL1 and SBL2 may have the same electric characteristics (parasitic resistance and parasitic capacitances)* and sub-source lines SSL1 and SSL2 may have the same electric characteristics. Owing to these dummy transistors DG1-DG4, the layout of transistors in memory cell unit MU can be symmetrical with respect to main bit line MBL, so that the layout can be made simple, and an influence by misalignment of a mask in a manufacturing process can be cancelled. By arranging the source line between the source select signal lines, the size of the unit in the column direction can be reduced." [Emphasis added].

From those cited paragraphs above:

(1) Dummy transistor DG2 turns on/off in response to drain-side block *select signal* SD2, therefore it is seen as a selection device.
(2) Dummy transistor DG2 *is selected* for equalizing the electric characteristics between selected sub-bit line SBL2 and unselected sub-bit line SBL1, therefore, it is seen as a selection device.
(3) Examiner agrees with Applicants' argument that dummy transistor DG2 does not coupled memory cells within the NAND string to some kind of memory array node. However, the claim language, especially claim 1, merely calls for first and second groups of control signals, *not the*

selection devices, to couple a series connected string of memory cell within the NAND string to the global array line and bias node.

The similar situation is present for DG4.